CLAIMS

We claim:

1. A method of forming a semiconductor device, comprising:

providing a substrate having a gate stack on the surface of the substrate;

forming an etch resistant liner over the gate stack;

forming a spacer over the liner along sidewalls of the gate stack;

removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer; and

forming a conductive material in the regions of the substrate and gate stack not covered by the liner.

2. The method of claim 1, further comprising before forming the liner over the gate stack:

providing a second gate stack on the surface of the substrate.

3. The method of claim 2, further comprising:

forming the liner over the second gate stack; and

forming the spacer over the liner along sidewalls of the second gate stack.

4. The method of claim 3, further comprising before removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer:

depositing a photoresist layer over the liner and the spacer of the second gate stack to prevent removal of the liner from the second gate stack.

5. The method of claim 3, further comprising after removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer:

forming an insulative layer on the surface of the substrate that covers the second gate stack before forming the conductive material.

6. The method of claim 2, further comprising before forming the liner over the gate stacks:

forming a first spacer along the sidewalls of the first and second gate stacks.

7. The method of claim 2, wherein the gate stack comprises a transistor gate stack and the second gate stack comprises a resistor gate stack.

8. The method of claim 1, wherein the liner comprises a material selected from the group consisting of: Al_2O_3, HfO_2, and Ta_2O_3.

9. The method of claim 1, wherein the liner comprises SiC.

10. The method of claim 1, further comprising before forming the conductive material in the

regions of the substrate and gate stack where the liner was removed:

performing a preclean process on the surface of the substrate.

11. The method of claim 1, wherein the liner comprises a material having a dielectric constant in the range of about 7-150.

12. The method of claim 1, further comprising during forming the conductive material:

forming source and drain regions within the substrate, wherein a location of the source and drain regions is determined by an end of the liner created by removing the liner from regions not covered by the spacer.

13. A method of forming a semiconductor device, comprising:

providing a substrate having a first gate stack and a second gate stack on the surface of the substrate;

forming a liner over the first and second gate stacks;

forming a spacer over the liner and along the sidewalls of the first and second gate stacks;

removing the liner from regions of the substrate and gate stacks not covered by the spacer;

forming a protective layer over the second gate stack; and

forming a conductive material in the regions not covered by the liner.

14. The method of claim 13, further comprising before forming the liner over the first and second gate stacks:

forming a first spacer along sidewalls of the first and second gate stacks.

15. The method of claim 13, further comprising before removing the liner from regions of the substrate and gate stack not covered by the spacer:

depositing a photoresist layer over the liner and the spacer of the second gate stack to prevent removal of the liner from the second gate stack.

16. The method of claim 13, further comprising before forming the conductive material:

forming an insulative layer over the second gate stack; and

performing a preclean process on the subsbtrate.

17. The method of claim 13, wherein the liner comprises an etch resistant material.

18. The method of claim 13, wherein the liner comprises a material selected from the group consisting of: Al_2O_3, HfO_2, and Ta_2O_3.

19. The method of claim 13, wherein the liner comprises SiC.

20. The method of claim 13, wherein the liner comprises a material having a dielectric constant in the range of about 7-150.

21. The method of claim 13, further comprising during forming the conductive material:

forming source and drain regions within the substrate, wherein a location of the source and drain regions is determined by an end of the liner created by removing the liner from regions not covered by the spacer.

22. A semiconductor device, comprising:

a gate stack formed on a substrate;

an etch resistant liner covering sidewalls of the gate stack and a portion of the substrate adjacent the gate stack;

a spacer on the liner along the sidewalls of the gate stack; and

a conductive material within a top region of the gate stack and within source and drain regions of the substrate, wherein the source and drain regions are located where the liner ends on the substrate.

23. The semiconductor device of claim 22, wherein the liner comprises a material having a dielectric constant in the range of about 7-150.

24. The semiconductor device of claim 22, wherein the liner comprises a material selected from the group consisting of: Al_2O_3, HfO_2, and Ta_2O_3.

25. The semiconductor device of claim 22, wherein the liner comprises SiC.

26. A semiconductor device, comprising:

a transistor gate stack and a resistor gate stack formed on a substrate;

a first spacer along sidewalls of the transistor and resistor gate stacks;

a liner over the first spacer of the transistor and resistor gate stacks, and along a portion of the substrate at a base of the transistor and resistor gate stacks, wherein the liner extends along the substrate to a designated location of transistor source and drain regions;

a spacer on the liner along the sidewalls of at least the transistor gate stack; and

a conductive material within a top surface of the transistor gate stack and within the transistor source and drain regions.

27. The semiconductor device of claim 26, further comprising:

a protective layer covering the resistor gate stack and the portion of the substrate at the base of the resistor gate stack.

28. The semiconductor device of claim 26, wherein the liner covers the entire resistor gate stack and the portion of the substrate at the base of the resistor gate stack.

29. The semiconductor device of claim 26, wherein the liner comprises a material having a dielectric constant in the range of about 7-150.

30. The semiconductor device of claim 26, wherein the liner comprises a material selected from

the group consisting of: Al_2O_3, HfO_2, and Ta_2O_3.

31. The method of claim 26, wherein the liner comprises SiC.